



# Velocity CAE<sup>®</sup> Program Generator

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For **Simulation to ATE** and  
**ATE to ATE Conversion**

Release 6.8.2

# Configuration Guide

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# Velocity CAE Program Generator Configuration Guide

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- 
1. In the **PINS** definition:
    - a. The symbols *pinList*, *startStopList*, *condition*, and *map* are high-level syntactical elements that are subsequently broken down into smaller elements.
    - b. The use of regular style square brackets around *condition* and *map* means that they are optional.
  2. In the *pinList* definition (*pinList ::=*):
    - a. The symbol *pinList* is defined as a comma-separated list of elements in which each element can be either a *pinName* or a *groupName*.
    - b. Note the use of the regular style vertical bar to indicate a choice of either *pinName* or *groupName*.
    - c. Note the use of the regular style braces to indicate 0 or more additional *pinName* or *groupName* elements, each preceded by a required comma.
    - d. The fact that the first occurrence of *pinName|groupName* is not enclosed in square brackets or braces means that at least one element must be specified. Any others are optional.
  3. In the *condition* definition (*condition ::=*):
    - a. The use of bold style braces means that braces are to be typed as a required part of the syntax.
  4. In the *conditionList* definition (*conditionList ::=*):
    - a. Note that the symbol *relativeCycle* is enclosed in two sets of square brackets.
    - b. The innermost brackets are in bold font, indicating that square brackets are to be typed as a required part of the syntax.
    - c. The outermost brackets are in regular font, indicating that the element within is optional.

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# CONFIGURATION GUIDE

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# 1.0 GENERAL INFORMATION

*A brief look at what a Velocity CAE configuration file entails and how it is create and used.*

## 1.1 What is a Configuration File?

A Configuration File is a human-readable, ASCII text file used by Velocity to control the conversion process.

Some of the aspects of the conversion process that a Configuration File controls are:

- The directory into which files generated by the conversion are to be written
- The period by which a VCD pattern is to be divided into cycles
- The target pin list, including test system resource assignments
- Pin groups
- Custom timing
- Custom levels
- Rules for creating custom patterns from existing patterns
- Standardized test and power up/down definitions
- Test flow

Every Velocity conversion – whether the ShellConstructor or Design-to-Test (D2T) or Tester-to-Tester (T2T) – requires the use of a Configuration File.

If the user does not specify a Configuration File and attempts to run a conversion, Velocity will display the following error message:



Configuration Files can be given any name, within the limitations of the host operating system. But, all names use a .cfg extension. They can reside in any directory that the user chooses.

## 1.2 Creating a Configuration File

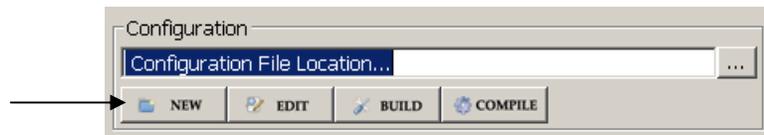
As a human-readable, ASCII text file, a Configuration File can be created and edited using any text editor. The user may choose to start from nothing and create the entire Configuration File in the text editor; or, use an existing file as a template and edit those elements which differ.

As an alternative, Velocity offers a way to speed up the Configuration File creation process. The Velocity GUI can quickly and automatically generate an initial Configuration File from an existing pattern file that is to be converted.

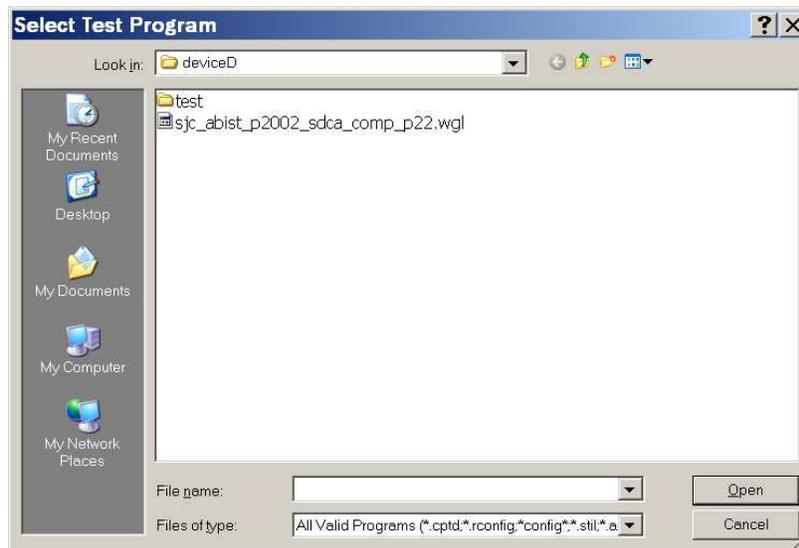
The automatic process will create a file containing, at a minimum, the definition of the target file path and the pin list. The user can then add any other required elements in the text editor.

### 1.2.1 Automatically Generating an Initial Configuration File

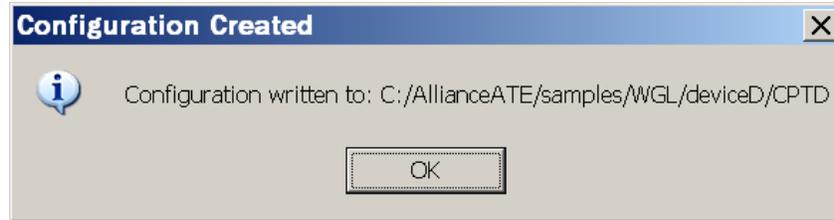
- From the GUI Configuration menu, select New.



- A window similar to the following will appear.



- Navigate to the directory containing the simulation output files or ATE files from which you want to build a test program.
- Select any one file which, at a minimum, defines all of the required pins to be used in the test program.
- Click the Open button. A progress indicator window will pop up, following by a completion message, similar to the one shown next:



- Note the location of the new Configuration file, as shown in the message. Click the OK button to acknowledge.

## 1.3 What Happens During the Conversion Process?

In order to better understand the aspects of the pattern conversion process that are controlled by the Configuration File, it is useful to have a basic understanding of what happens during conversion.

### 1.3.1 Conversion Process Inputs

Every Velocity conversion takes, as input, one or more pattern files of one of the following supported types:

- STIL
- VCD/EVCD
- WGL
- VCT
- CPTD (Credence ASL3000)
- XLS/ATP (Teradyne J750)
- XLS/ATP (Teradyne UltraFlex)
- ADR (Teradyne J973)
- AVC/DVC (Advantest 93000)

### 1.3.2 “Cyclized” vs. “Uncyclized” Pattern Formats

ATE test systems output functional stimulus to the device (and sample functional responses from the device) in the form of a vector sequence. The vectors are presented at a particular rate defined by the **cycle time** (also known as the **period**).

The following are excerpts from a STIL pattern file and timing file, respectively, showing how digital pattern sequences and corresponding cycle timing are represented in an ATE environment:

```

////////////////////////////////////
//  Pattern Block: example_vectors
////////////////////////////////////
Pattern example_vectors {
Start_example_vectors:
    W "tps66000_10000";
    V { all = 0XXXXXXXXXXXXXXXXXXXXX00XXXXXX1XXXXXXXX1XXXXX0X00X00XXXX1X; }
//0
    V { all = 0XXXXXXXXXXXXXXXXXXXXX00XXXXXX1XXXXXXXX1XX0XX0X00X00XXXX1X; }
//1

```

```

////////////////////////////////////
//  Timing Blocks
////////////////////////////////////
Timing "customTiming" {
    WaveformTable "tps66000_10000" {
        Period 'PERIOD';
        Waveforms {
            "addr[10]" {
                01Z { '0.000*PERIOD' D/U/Z; }
                LXXM { '0.091*PERIOD' L/H/X/T; }
            }
            "addr[11]" {
                01Z { '0.000*PERIOD' D/U/Z; }
                LXXM { '0.091*PERIOD' L/H/X/T; }
            }
        }
    }
}

```

Many other simulation and test data formats, such as WGL (Waveform Generation Language), also have a concept of vectors and cycle times, which can be translated to tester independent STIL format in a relatively straightforward manner. These kinds of pattern formats can be categorized as **cyclized** formats.

The following are excerpts from a WGL file, showing how digital pattern sequences and cycle timing, corresponding to the STIL example above, are represented in a WGL format:

```

pattern Chain_Scan_test("extal", "dft_setup", "dft_atpg", "dft_shift",
...
{ Pattern 0 Cycle 0 Loop 0 }
vector(+, tps66000_10000) := [ 0 0 0 0 0 0 0 0 - - - - - - - - - -
...
{ Chain_test }

```

```

    { Pattern 0 Cycle 1 Loop 1 }
    { Begin chain test }
repeat 6      vector(+, tps66000_10000) := [ 0 1 0 0 0 0 0 - - - - -
--

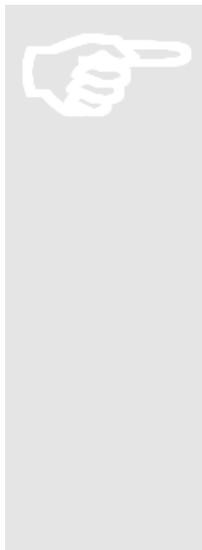
```

```

timeplate tps66000_10000 period 66000ps
...
"addr[10]" := input[0ps:S];
"addr[11]" := input[0ps:S];
...
"addr[10]" := output[0ps:X, 6000ps:Q'edge];
"addr[11]" := output[0ps:X, 6000ps:Q'edge];

```

OBSERVATIONS:



1. In the above comparison of STIL and WGL formats, the pins were not defined in the same order; so, the vector columns will not match up. However, the same underlying vector data, per pin, would be contained in each format.
2. In the STIL example on the previous page, note how vectors and cycle timing are brought together by preceding a sequence of vector lines (those lines that begin with “V”) with a waveform table selection line beginning with “W”. The waveform table specified after the “W” is defined within the Timing Block shown on the same page.
3. In the WGL example above, cycle timing is defined within a **timeplate** definition, and then brought together with vectors in individual vector lines (those lines containing the keyword **vector**), by referencing the **timeplate** name.

Not all pattern formats are cyclized. The most notable examples of **non-cyclized** formats are the VCD (Value Change Dump) and EVCD (Extended Value Change Dump) formats. In these non-cyclized formats, signal patterns are represented as a continuous stream of events, where an event is a change of state at a particular point in time relative to the beginning of the pattern.

The following is an excerpt from an example VCD file:

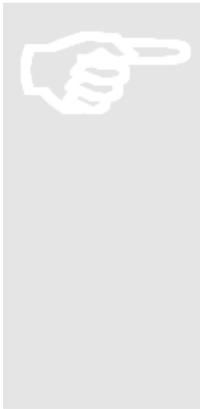
```

...
#1000
pT 0 0 <262
pT 0 0 <263
pX 6 0 <265
pX 6 0 <266
pL 6 0 <267

#3000

```

pb	6	6	<9
pb	6	6	<10
pb	6	6	<11
pb	6	6	<12
#4000			
pN	6	6	<96
pN	6	6	<97
...			



### OBSERVATIONS:

1. The lines beginning with “#” are timestamps, with the time unit being specified previously in the file with the \$timescale statement. (In this example, the time unit is 1ps; so, 1000 represents 1ns.)
2. Following each timestamp line is a sequence of value change lines, one for each signal which changes state at that timestamp. (Signals which do not change state at that timestamp are not listed.)
3. The first field of each value change line is the state to which the signal changes. The fourth field is an arbitrary, user-defined symbol for a specific signal.

For VCD, Velocity will analyze the spacing of timing events for each signal, and determine a best-fit tester cycle time and edge delays for your test program.

## **2.0 CONFIGURATION FILE STRUCTURE**

*Information on the structure and syntax of a Velocity Configuration File.*

## 2.1 Syntactic Elements

Configuration Files are made up of a number of different types of syntactic elements.

At the top level, there are two main types of elements. These types are:

- **Control Definitions**, which define particular aspects of the conversion and program generation process; and,
- **comments**, which begin with the '#' symbol and continue to the end of the line.

## 2.2 Control Definitions

Control Definitions can be categorized into two forms: **single-line** and **multi-line**.

### 2.2.1 Single-line

A single-line definition begins with a **keyword**, includes one or more **parameters**, and continues to the end of the line or to the beginning of a comment, whichever comes first.

The following **PERIOD** definition is an example of a single-line Control Definition:

```
PERIOD      5.000ns default
```

In this example, the keyword is **PERIOD**, and the two parameters are **5.000ns** (the value of the target period for cyclization) and **default** (the name given to this particular target period, or *Clock Domain*).

### 2.2.2 Multi-line

A multi-line definition (also called a **block**) consists of a **starting line**, zero or more **sub-parameter lines**, and an **ending line**.

- **Starting Line**

The starting line begins with a **keyword** and includes zero or more **parameters**.

- **Sub-parameter Line**

A sub-parameter line consists of one or more keywords and/or user-defined symbols or values whose order depends on the type of Control Definition. Each line provides further details in the definition of the Control.

- **Ending Line**

The ending line consists of the keyword **END** followed by the starting line keyword.

The following **PINLIST** block definition is an example of a multi-line Control Definition:

```
PINLIST
    ANALOG_VDD          default IO    ANALOG_VDD
    CVDD                default IO    CVDD
    HOLDn              default IO    HOLDn
END PINLIST
```

Note that the block begins with a starting line consisting only of the keyword **PINLIST** and ends with an ending line consisting of **END PINLIST**. In between are sub-parameter lines that begin with a pin name and consist of several parameters that define properties of the pin.

### 2.2.3 Comments

Comments can appear anywhere within the Configuration File, with the following restrictions:

- They only extend to the end of the line. Multi-line comments require a separate starting “#” for each line.
- Everything from the starting “#” to the end of the line is part of the comment. No part of a Control Definition will be recognized by Velocity if placed after the “#”.
- If a comment is placed at the end of a Control Definition line, the starting “#” must be separated from the last Control Definition line character by whitespace. (See below for more information on the use of whitespace in Configuration Files.)

The following is an example of a multi-line comment in a Configuration File, with the comment on each line taking up the entire line:

```
#####
## PinList Definition
#####
```

The following is an example of a comment at the end of a Control Definition line (in this case, the starting line of a TEST definition block):

```
TEST contNegative 150 # Continuity test with negative forcing current
```

### 2.2.4 Keywords

Keywords are Velocity reserved words. That is, they may not be used for user-defined names, such as ClockDomain names, Pin names, and Pattern names.

Keywords are NOT case-sensitive. For example, Velocity would interpret **period** the same as **PERIOD** or, even **pErIoD**. However, for readability purposes and for establishing a standard convention, it is recommended that all keywords be in **UPPER-CASE**.

### 2.2.5 Parameters

Parameters are elements of a Control Definition that allow the user to provide details for a particular instance of the Control. The user does so by giving a user-defined symbol or value, called an **argument**, at the corresponding parameter location.

For example, the first parameter in the starting line of the TEST block definition is the test name. In the example above, the argument for that parameter is “contNegative”.

Arguments for parameters ARE case-sensitive. So, a later test flow definition referencing the TEST called “contNegative” would have to specify the exact same case.

### 2.2.6 Use of Whitespace

Whitespace in a Configuration File includes spaces and tabs.

A Configuration File may contain any amount of whitespace at the beginning and end of lines, and between keywords, parameters, and comments. Some parameters, such as the pin list of a PINS masking definition, can be specified with multiple sub-elements separated by a non-whitespace character. The following example shows a PINS sub-parameter definition within a PATTERN block definition:

```
PATTERN func pat_masked
  PINS Q0,Q1,Q2,Q3 55-83
END PATTERN
```

Note that the pin list, “Q0,Q1,Q2,Q3”, is considered the argument to one parameter of the PINS definition. Therefore, it contains no embedded whitespace. The individual sub-elements (Pins in this case) are separated only by commas. Likewise, the cycle range parameter is made up of a start and stop address separated by a hyphen.

## **2.3 Line-Oriented Structure**

The main elements of a Configuration File – Control Definitions and Comments – follow, for the most part, a line-oriented structure. That is, the end-of-line (i.e. carriage return) marks the end of:

- Single-line Control Definitions;
- Starting and Ending lines of Multi-line Control Definitions;
- Sub-parameter lines of Multi-line Control Definitions (with exceptions noted below); and,
- Comments.

The only exceptions to the end-of-line termination are the masking sub-parameter definitions – ON, OFF, and PINS – of a PATTERN block definition. Those sub-parameter definitions are terminated by a semicolon (;) and are allowed to extend to multiple lines. This feature allows for long, complex masking definitions. Refer to the detailed description of the PATTERN block syntax later in this guide.

Also, as noted in the previous section of this guide on Comments, a Control Definition line may be terminated by the beginning of a Comment on the same line.

## 2.4 List of Control Types

The following table lists all of the available Control Types for a Configuration File, along with a brief description.

Control Type	Description
<b>PATH</b>	Base directory path for test program files
<b>DEVICE</b>	Sub-directory of path specified by PATH Control, used to hold test program files for a specific device
<b>PROGRAM</b>	Base file name used for various timing, levels, and pattern files and subdirectories
<b>SOURCE_PORT</b>	Default value for the Source port. This will cause the source port to be automatically defined when the Configuration File is loaded. Valid entries can be chosen from anything that is present in the Source Port drop down list in the GUI.
<b>TARGET_PORT</b>	Default value for the Target port. This will cause the target port to be automatically defined when the Configuration File is loaded. Valid entries can be chosen from anything that is present in the Target Port drop down list in the GUI.
<b>PERIOD</b>	Specifies the time period used for “cyclizing” a VCD or EVCD pattern, per “Clock Domain”
<b>EDGES</b>	Specifies maximum number of timing edges to expect within a tester period
<b>PINLIST</b>	Assigns type and tester resource to each active Pin
<b>MODEL</b>	(Advantest 83K- and 93K-specific) Specifies tester model
<b>MEMORY</b>	(Advantest 83K- and 93K-specific) Type of pattern memory to use
<b>METHOD</b>	(Advantest 83K- and 93K-specific) Type of test method to use
<b>SUBROUTINE</b>	Defines whether pattern subroutines from source will be flattened in-line with the calling pattern, or kept as a separate, called pattern
<b>MACROSTYLE</b>	For STIL sources
<b>PERSISTENCE</b>	Specifies whether Velocity samples a VCD file for a short or a long portion for calculating a best-fit cyclization period

<b>UNDERSAMPLE</b>	Specifies a strobe interval, N, to apply to a converted pattern, in which only every Nth cycle can have output strobes, and intervening cycles will be masked
<b>DELAY</b>	Assigns cycle delay to pins listed
<b>PATTERN</b>	Defines a custom pattern modified from an existing pattern
<b>TIMING</b>	Defines custom timing for a set of Pins to override the timing derived from the input files
<b>LEVELS</b>	Defines DC levels for a set of Pins to be used in the test program
<b>POWER</b>	Defines a power up or power down sequence
<b>TEST</b>	Creates a specific instance of a standardized test type
<b>FLOW</b>	Defines a sequence of previously-defined TEST instances to be inserted into the test program
<b>TERM</b>	Defines the beginning of termination block that can be used to Set the drive action for comparisons on IO pins

## 2.5 Order of Control Definitions

Many of the Control Definitions can reference elements that are defined in other Control Definitions elsewhere in the Configuration File. For example, a TIMING block definition can reference a Pin defined in the PINLIST block or a Group defined in a GROUP definition.

Elements must be defined in a Configuration File before they can be referenced. Therefore, the order of Control Definitions within the file is important. The order of the Control Types shown in the previous table is the recommended order in which those types should be defined.



**NOTE:** It is not necessary to define every Control Type in a Configuration File. Velocity uses a default set of properties and behaviors for those aspects of a conversion not defined in the Configuration File. Only those Control Types with properties which differ from the defaults need to be defined.

## 2.3 Example Configuration File

The following simple Configuration File example includes definitions from each of the Control Types:

```
#####
#
# ASCII Velocity Configuration File
#####
#
PATH /home/field/testPrograms
DEVICE 56374
PROGRAM ShellExample

#####
# PIN LIST: This will define regular IO and power pin defs
#####
PINLIST
    p0          default          I      0 11
    p1          default          I      0 83
    q0          default          O      0 69
    q1          default          O      0 76
    cpd         default          CLK    0 62
    cpu         default          CLK    0 55
    VS1        DPS              POW    4 0
END PINLIST

GROUP   clocks = "cpu,cpd"

#####
# Pattern lists
#   The following patterns will be translated.  If the pattern is
#   not in the list, then it will be skipped.  If the pattern is
#   not in the source file then a warning will be issued.
#####
PATTERN multipleLoop
    BASE SpecFunc
    LOOP 5,10 16
END PATTERN

#####
# Timing and Levels
#   definitions will define the values of specs. The following
#   values will be assigned by default. Groups and pins can
#   be defined to override defaults by using a pin name or group
#   name.
#####
TIMING default
    period 100ns
```

```

offset 0ns
duty 50%
drive 25%
receive 90%
END TIMING
LEVELS default
POWER 3.3V
VIL 10%
VIH 90%
VOL 40%
VOH 60%
END LEVELS

#####
# Power up and power down
#####
POWER nominal
VS1 1.25V 500mA 5uS
END POWER

#####
# Test Definitions
# The following tests will be defined as discrete functions
# that can be executed as user commands or as part of flows
#####
TEST contNegative 150
TYPE cont
FORCE -10uA
CLAMP 2V
LOW 400mV
HIGH 800mV
PINS ALL
END TEST
TEST funcSpec 1
TYPE func
PATTERN SpecFunc
END TEST

#####
# Flow Definition
# The following tests will be executed in the following
# order. If no flow is defined, then all the tests will
# be included in the order they are defined.
#####
FLOW experimentName
TEST contNegative
POWER nominal
TEST funcSpec
DELAY 15ms
POWER off
END FLOW

```

## **3.0 CONTROL DEFINITION REFERENCE**

*Definitions and examples for all configuration file variables and blocks*

## 3.1 Environment Definitions

The Environment section of the Configuration File consists of a set of definitions that define the location and naming of the target test program files. Typically, this is the first section in a Configuration File.

Velocity divides the test program location and file names into three parts:

- base path – Typically, points to the directory used as the parent directory of all test programs.
- Device name – Appended to the base path. Categorizes test programs by device.
- Program name – Specifies a base file name that Velocity will use for many of the generated test files. (Pattern files for the target tester are typically named for the source pattern files.)

The test program directory path and file names are defined by the following Control Types:

- **PATH**
- **DEVICE**
- **PROGRAM**

### 3.1.1 PATH

*Syntax:*

**PATH** *pathName*

where,

*pathName* is a directory path specifier

*Example:*

```
PATH /home/programs
```



**NOTE:** The directory path specifier must use valid syntax for the underlying file system.

### 3.1.2 DEVICE

*Syntax:*

**DEVICE** *directoryName*

where,  
*directoryName* is the name of a directory

*Example:*

```
DEVICE      coolChip
```

### 3.1.3 PROGRAM

*Syntax:*

**PROGRAM** *fileName*

where,  
*fileName* is the base name to be used for generated test files

*Example:*

```
PROGRAM      finalTest
```



Using the PATH, DEVICE, and PROGRAM Definitions in the above examples, Velocity would create test program files for the Build under the directory

**/home/programs/coolChip**

A number of the created test files would begin with base file name **finalTest**. Their location under the device directory (or subdirectories thereof) would depend on the specific target test system.

## 3.2 General Build Definitions

The General Build section of the Configuration File consists of a set of definitions that define the basic settings common to any conversion.

### 3.2.1 SOURCE\_PORT Definition

Specifies the Source Port for the Velocity conversion. Valid entries can be chosen from anything that is present in the Source Port drop down list in the GUI.

*Syntax:*

**SOURCE\_PORT** *sourcePortType*

where,

*sourcePortType* is a valid licensed source entry.

*Examples:*

```
SOURCE_PORT WGL
```

```
SOURCE_PORT VCD
```



**NOTE:** The source type must match a valid licensed entry or this variable will be ignored.

### 3.2.2 TARGET\_PORT Definition

*Syntax:*

**TARGET\_PORT** *targetPortType*

where,

*targetPortType* is a valid licensed target entry. Valid entries can be chosen from anything that is present in the Target Port drop down list in the GUI.

*Examples:*

```
TARGET_PORT STIL
```

```
TARGET_PORT 93K
```



NOTE: The target type must match a valid licensed entry or this variable will be ignored.

### 3.2.3 LIBRARY

This variable is used to define the name and location of any predefined libraries that you want to have included in the target program

*Syntax:*

```
LIBRARY   EXTERNAL|LOCAL LIBRARY_FILE_NAME
```

where,

**EXTERNAL|LOCAL** directs Velocity whether to physically copy this library to the target program or simply refer to its path through a makefile or some other method depending on the target.

*LIBRARY\_FILE\_NAME* is the path and name of the library file itself

*Examples:*

```
HEADER      LOCAL /usr/local/lib/someLibrary.so
HEADER      EXTERNAL  /usr/local/lib/ someLibrary.so
```



NOTE: referenced library file must be present and valid for the target

### 3.2.4 HEADER

This variable is used to define the name and location of any predefined headers that you want to have included in the target program

*Syntax:*

```
HEADER    EXTERNAL|LOCAL HEADER_FILE_NAME
```

where,

**EXTERNAL|LOCAL** directs Velocity whether to physically copy this header to the target program or simply refer to its path thro a makefile or some other method depending on the target.

***HEADER\_FILE\_NAME*** is the path and name of the header file itself

*Examples:*

```
HEADER    LOCAL /usr/local/include/someHeader.h
HEADER    EXTERNAL    /usr/local/include/someHeader.h
```



NOTE: referenced header file must be present and valid for the target

## **3.3 Pin Configuration Definitions**

### **3.3.1 PINLIST Definition**

*Syntax:*

**PINLIST**

*pinName*            *domain* *pinType* [*slot*] [*channel*] [*alias1* [*alias2*...*aliasN*]]

**END PINLIST**

The PINLIST block defines, per pin, the tester channel assigned and any alternate versions of that name used in the simulation or ATE conversion source.

The tester channel information that can be specified includes:

- domain:
  - **For digital pins:** default or any port name that does not have a n underscore)
  - **For power supplies:** DPS16, DPS32, UHC4, MSDPS (type must be POW)
- *pinType*. **I, O, IO, CLK, REF, POW, R, DIR, A,** or **NC**. (See the *Velocity Program Generator User's Guide* for more information on these types.)
- Slot number
- Channel number
- The alternate pin names are known as Aliases. You can specify as many Aliases on a pin line – separated by whitespace – as you need. Velocity uses Aliases to match simulation or ATE pin names that are different from the target pin name.

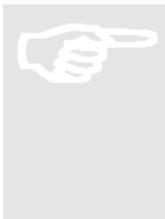
The following is an example of a PINLIST definition:

```
#####
##  PinList Definition
#####
PINLIST
    ANALOG_VDD          DPS16    POW    230    2
    HOLDn               default   I     101    1  hold_n holdn
    WPn                 default   O     101    8  wp_n
    anapadext_data_n   DPS16    POW    230    3
END PINLIST
```



Pin ANALOG\_VDD uses channel 2 of a DPS16 card in slot 230.

Also, note that pin HOLDn has aliases of hold\_n and holdn, meaning that it can take its data from simulation or ATE conversion sources that use either of those alias names.



If a Relay pin is defined, this also assumes that it is using a default type

### 3.3.2 BIDIRECTIONAL CONTROL

One special case within the PINLIST section is the bidirectional control pin. A control pin will only be needed for standard VCD translations. This source port format does not have a state character differentiation between input and output. Therefore, without the extra control wire, there is no way to determine the IO state of a bidirectional pin. For these types of simulations, there must always be a set of control wires that would also be included in the VCD file. These are “virtual” pins that are used to define the IO direction of other pins. In other words, these pins are controls for other pins.

The Velocity configuration syntax for these is similar to the regular pins except the alias column would be used to make reference to another pin instead of merely providing an alternate name for the active pin. There will then be two rows used to define each bidirectional pin. One for the pin itself, and another for the control wire defining its IO state. Once this is defined the control wire’s state is kept as the VCD file is processed. At any given time, if the control pin is actively high, then the pin which it controls is set to output mode. If the control wire is low, then the pin which it controls is set to input mode.

Example

DATA0	default IO	data[0]
DATA1	default IO	data[1]
DATA2	default IO	data[2]
DATA3	default IO	data[3]
control0	default DIR	DATA0
control1	default DIR	DATA1
control2	default DIR	DATA2
control3	default DIR	DATA3

In the above example, there are 4 pins defined as IO and 4 pins defined as DIR. For the IO pins, there is an alias that defines an alternate nomenclature that the simulation file might use to express the given pin name. For the DIR pins, the alias column contains an entry that is already defined as a column 1 pin name. This pseudo-alias is the key that provides the connection between the control pin and its target.

The pin listed as DIR type will not show up in the target test pattern. These are treated as virtual pins rather than real pins that would require data to be provided behind them.

As stated above, the default behavior for control pins is that a control pin high means output mode. Control pin low means input mode. This behavior can be inverted by also inserting the keyword “NEG” at the end of the control pin definition (after the alias). If the NEG keyword is used, then the convention will be opposite. Control pin high will indicate input mode. Control pin low will indicate output mode.

Example

DATA0	default IO	data[0]
control0	default DIR	DATA0 NEG

### 3.3.3 GROUP Definition

The GROUP Control definition allows you to assign a name to a group of pins, for easier reference elsewhere in the Configuration file.

To define a Group, use the keyword **GROUP** followed by a Group name, followed by an equals sign (=) and a comma-separated list of pin names enclosed in double-quotes (""). The following is an example of a Group definition:

```
GROUP DBUS = "D0, D1, D2, D3, D4, D5, D6, D7"
```



If you use a group as a member of another group, this group must have already been defined. If not already defined a configuration loader error will occur.

### Automatic Group definitions

There are a number of groups that are automatically generated. These groups are generated automatically because certain APIs assume that they are there. For example, the functional test API does an automatic connect on all pins. This assumes that there is a group named “allpins” that is there and this group’s contents include all of the digital pins for a given device.

<b>Automatic Group Name</b>	<b>Description of Contents</b>
<b>allpins</b>	All digital pins not including any trigger pins that may be assigned
<b>allios</b>	All bidirectional pins
<b>allins</b>	All pins that can have input actions. Includes bidirectionals as well as input only pins
<b>allouts</b>	All pins that can have output actions. Includes bidirectionals as well as output only pins
<b>triggerPins</b>	Group to collectively define all trigger pins
<b>Allpins</b>	All digital pins including the trigger pins. This is used to connect and disconnect all pins.
<b>allSupplies</b>	All DPS defined power pins

## 3.4 Source-Port-Specific Variables

The Source-Port-Specific section of the Configuration File consists of a set of definitions that define build settings specific to the selected Source Port.

### 3.4.1 IGNORE TIMEPLATE

Sometimes WGL files have timeplates that the user wants to ignore like at the start of a simulation. You can instruct Velocity to ignore these timeplates.

**IGNORE TIMEPLATE** timeplatename

### 3.4.2 JOB

This directive is used to enable a specific job as defined in a J750 or UltraFlex source test program. This feature is ignored for all other input ports. When used, the active spec sheets for timing and levels are picked from a specific job. If the job does not exist in the source, by a typo or any other reason, the last job is always the one that is chosen. This is also what is chosen when no JOB is defined at all.

*Syntax:*

**JOB** *jobName*'

*Example:*

```
JOB          QA_TEST
```

### 3.4.3 MACROSTYLE

This variable will allow you to tell velocity how to interpret Macros and Procedure when loading STIL simulation files. Depending on the way these are created variables to pass values into subroutines will either be passed through STIL Macros or with STIL procedures. It will be one or the other but not both. By default these are done with Macros. Therefore, therefor the default value for this flag is "1". But, if your source STIL files pass variables into procedures instead, you can handle this by disabling the passed variable usage in the macros by setting the MACROSTYLE flag to "0"

*Syntax:*

**MACROSTYLE** 0|1

*Example:*

```
MACROSTYLE    0    # Procedures pass variables
MACROSTYLE    1    # Macros pass variables (This is default behavior)
```

### 3.4.4 MASTER

When using any of the EVCD format, there may be places where the state characters that are used indicate that the bench and the DUT are both driving. If not specified, Velocity will take the DUT as the master. That means that the competing drive values will result in the DUT value being used instead of the bench. If you specify the bench as the master, the opposite will occur. EVCD state characters of “0” or “1” will then be assumed to be tester drives instead of tester strobe values.

*Syntax:*

**MASTER** *DUT|BENCH*

*Example:*

MASTER	DUT
MASTER	BENCH

### 3.4.5 PERSISTENCE

By default, a very small portion of a VCD file is used to evaluate the pins and calculate periods. Sometimes this is insufficient when multiple time domains are active. One domain may start toggling later than another. For this reason, there may not be enough actions in one domain to properly calculate a period. If this is the case, the user will receive a message that informs them that PERIOD values for one domain will track with the other. If this is undesired there is a secondary calculation scheme that might work. This is called “PERSISTENCE” mode. If enabled, a much larger page size will be used to calculate periods.

This is disabled by default, but can be explicitly assigned with the following syntax.

*Syntax:*

**PERSISTENCE** *ON|OFF*

*Example:*

PERSISTENCE ON	# persistence is enabled
PERSISTENCE OFF	# persistence is disabled

### 3.4.6 UNDERSAMPLE

This allows you to apply a global value that will block strobes except in cycles with a clean modulus to whatever is specified here. When OFF, all cycles are strobed.

NOTE: This is called UNDERSAMPLE instead of OVERSAMPLE because we are telling Velocity to undersample by a particular factor. The action applied by Velocity is undersampling. The source file itself may be oversampled. But, this action is applying itself to the translation process. Therefore it is called UNDERSAMPLING here.

**UNDERSAMPLE** OFF # No undersampling

**UNDERSAMPLE** 5 # Under sample by a factor of 5.

## 3.5 Target-Port-Specific Variables

The Target-Port-Specific section of the Configuration File consists of a set of definitions that define build settings specific to the selected Target Port.

### 3.5.1 BINL

Compilation to the 93K will result in a pattern master file as well as a merged binary file. If you wish to include statistics in the compilation then you'll need to create the concatenated BINL file as well. This is enabled by turning BINL "ON"

*Syntax:*

```
BINARY ON|OFF
```

*Example:*

```
BINARY    ON      # merged BINL will be created
BINARY    OFF     # Only PMFL will be created
```

### 3.5.2 COMBINATION

Velocity dynamically builds a combination file base on your XMODE state. If the user want to tell Velocity to use a specific combination file, here is the syntax. This is specific to the 93K testers.

*Syntax:*

```
COMBINATION fileName
```

*Example:*

```
COMBINATION    /home/demo/device/ACT74.cmb
COMBINATION    ACT74.cmb # This will look alongside the CFG file
```

### 3.5.3 CONFIGURATION VARIABLE

This variable allows for a pre-defined 93K pin file to be used for compilation purposes and for usage in all testflows that are created. If nothing is specified for this, then the pin file will be auto created from the PINLIST block of the CFG. This variable is useful if you are applying patterns to an existing program where you have created your pin file already and/or you want to use multi site.

```
CONFIGURATION myCfgName # velocity will use pre-defined pin file
```

### 3.5.4 CTIM

This variable will control whether or not timeset switching is allowed or not for the V93K. By default, CTIM's are disabled. These are disabled because this will result in either very long run times due to break cycles or will result in timing that is too large to compile. But, there are situations where this is the correct usage. So, this variable is present to enable such actions on the system

Syntax:

```
CTIM ON|OFF
```

*Examples*

```
CTIM ON
CTIM OFF
```

### 3.5.5 DOMAIN TRACKING

Domain tracker allows you to specify the timing relationship between ports. In the following example the device has three well defined ports: 1. CLOCK, 2. DDR and 3. SDR

*Syntax:*

**DOMAIN**

```
domainName MASTER|SLAVE [slaveDomainName [periodMultiple]]
```

where,

**domainName:** matches domains defined in PINLIST block

**MASTER|SLAVE:** determines whether the period is defined itself or dependent on another domain

**slaveDomainName:** If specified as a SLAVE, then this will refer to another port already defined as master

**periodMultiple:** defaults to 1.0, If other, then the current domain will track with the MASTER at the given period multiplier

*Example:*

**DOMAIN**

```
CLOCK MASTER # PortName MASTER(Reference)
DDR SLAVE CLOCK 1.0 # PortName SLAVE Port2Track Ratio
SDR SLAVE CLOCK 75 # PortName SLAVE Port2Track Ratio
```

**END DOMAIN**

### 3.5.6 FASTMODE

This directive is used to enable or disable the use of fastmode. Fastmode is an Advantest digital option that uses a software programmable switch to enable faster drivers. When this mode is used, special care will be taken in how the timing is exported. All pins that are set to toggle at a rate that is faster than 1.25ns will be set to use the FAST option. Data bit rates and all compilation and tester file options will automatically be adjusted. If nothing is specified, then this option is assumed to be OFF.

*Syntax:*

```
FAST ON|OFF
```

*Example:*

```
FAST      ON
```

### 3.5.7 FSPINS

This block specifically applies to the SmartScale series of cards for the Advantest V93000 tester. These channels have a property that allows the Z edges to be handled independently from the drive edges. This features allows for a zero turn around time setup for bi-directional pins. If any target other than V9300 coupled with a MODEL definition of PS6800 is used, then this block will be ignored.

*Syntax:*

```
FSPINS
  pinName1 | groupName1
  pinName2 | groupName2
  ...
  pinNameN | groupNameN
END FSPINS
```

This blocks serves as a container for a list of pins or groups that should be setup with timing in such a way that the drive and Z edges are separated. Any pin left off this list will be treated as a regular IO pin instead of a FAST IO pin.

*Example:*

```
FSPINS
  DQ
  MQ
COMBINATION
```

### 3.5.8 MEMORY

Compilation to the 93K can be done using Vector Memory or Sequencer Memory. By default, vector memory is used. If you want to only use sequencer memory you can override using this directive .

*Syntax:*

**MEMORY** *SM|VM*

*Example:*

```
MEMORY      SM      # sequencer memory
MEMORY      VM      # vector memory
```

### 3.5.9 METHOD

(Specific to the Advantest 83K and 93K ports.) Specifies the type of testmethod to be used: Classic (CTM) or Universal (UTM). Used for generating the appropriate format for the testflow file.

*Syntax:*

**METHOD** *CTM|UTM*

*Example:*

```
METHOD     CTM     # Classic Testmethod
METHOD     UTM     # Universal Testmethod
```

### 3.5.10 MODEL

*Syntax:*

**MODEL** *modelType*

where,

*modelType* is a tester model type. This Control is specific to the Advantest 83K and 93K tester ports. Valid entries are:

- F330
- C400
- P1000
- PS400
- PS800
- PS6800
- PS3600

*Examples*

```
MODEL      PS3600  # PinScale
MODEL      PS6800  # SmartScale
```

## 3.6 Verilog Feedback Variables

There are set of configuration commands blocks that are intended specifically to affect the export of Verilog feedback files. These variables will have no effect on regular ATE output files. If “Enable Verilog Feedback” is not checked in the GUI or enabled from the command line, then all of these variables will simply be ignored by the Build process.

### 3.6.1 MAXDELTA Definition

When Verilog feedback is enabled, there may be instances where delta values for timestamps may be too large for the compiler that will be used. By default, the maximum delta is 400us. If a delta is larger than this it will be broken into multiple timestamps and spread.

This directive can be used to use a different value other than 400uS.

If no units are specified the number will be assumed to be in ns.

*Syntax:*

**MAXDELTA** *value*[ps|ns|us|ms|s]

*Example:*

```
MAXDELTA    200us    # max delta of 200us
MAXDELTA    500000  # max delta of 500000ns
```

### 3.6.2 MODULE

This variable will define the `moduleName` that is to be used in the Verilog feedback files if that option is chosen. If not defined at all, the default for the `moduleName` variable in the testbench and EVCD files created will be “`moduleName`”. This allows you to tune it so that resims can happen more semmlessly.

*Syntax:*

**MODULE** *moduleName*

*Example:*

```
MODULE      hx_5672
MODULE      dsp_1080
```

### 3.6.3 VERILOG Definition

When using the Verilog feedback path, testbenches can have their timings expressed in one of two ways. Sequential timing will express all timestamps as relative deltas from the previous stamp. On large simulations these numbers can end up too large for the target Verilog compiler. Parallel will express each timestamp as its wall time clock value. This can result in very large numbers that may crash. By default, parallel timing is used.

*Syntax:*

**VERILOG** *SEQUENTIAL|PARALLEL*

*Example:*

VERILOG	SEQUENTIAL	# Express edges as delta from previous edge
VERILOG	PARALLEL	# express every edge as a unique timestamp

### 3.6.4 WINDOW

Verilog files are always print on change. In simulations, that means that only transitions are exported as timestamps. For input actions this is simple. For output actions, the ATE versions of the same stimulus will inherently insert Z-actions before each strobe. By default, these Z actions are left out of the Verilog files. If the user wants to add these actions in the “WINDOW” variable can be used to essentially define the length of the active strobe window. If WINDOW is OFF, as it is by default, then there will be no closing actions added to close the strobe windows.

In the end, this is a more exact representation of what the ATE is doing, however, the resulting verilog files will be much larger.

*Syntax:*

**WINDOW** OFF | *value[ps|ns|us|ms|s]*

*Example:*

WINDOW	OFF	# no windowing off output actions
WINDOW	20ps	# Use 20ps strobe window

### 3.6.5 FEEDBACK FILTER

Verilog feedback files will export all ATE actions in all cycles and on all pins by default. In some cases, the user may want to limit the export. This can be limited to a certain cycle range. It can be limited by certain pins. Or, you can choose to export certain pins as running clocks instead of explicit data. All of these actions are taken to limit the size and scope of testbench. FEEDBACK filter blocks can be created that can tune the verilog scope on a pattern by pattern basis

*Syntax:*

```
FEEDBACK default|patternName [start-stop]
    pinName1|ALL    ON|OFF|CLK
    pinName2    ON|OFF|CLK
    pinName3    ON|OFF|CLK
    ...
    pinNameN    ON|OFF|CLK
END FEEDBACK
```

**default|patternName:** name of feedback block. If the name is “default”, then this filter will apply to all patterns. If the name is something else, then the filter will only apply to patterns whose name matches that of the FEEDBACK block

**start-stop:** This is an optional field that can assign the start and stop location for the verilog files. If left off then ALL cycles will be exported. These times can be expressed in either picoseconds or as a percentage. If the “%” is used, then you can export just the segments you like as a percentage of time. It is important to realize that this percentage is relative to the time value as opposed to the physical file location.

**pinNameN|ALL:** pin name to be added as regular pin (ON), removed from Verilog files (OFF), or included in Verilog as a running clock (CLK)

Examples:

```
# Export Verilog on all cycles for all pins except data[0-2].
FEEDBACK default
    ALL ON
    data0 OFF
    data1 OFF
    data2 OFF
END FEEDBACK

# Export Verilog for patternA for the first 25% only. Include only CLK32
# expressed as running clock and data[0-2] expressed as regular data
FEEDBACK patternA 0%-25%
    CLK32    CLK
    data0 ON
    data1 ON
    data2 ON
END FEEDBACK
```

## **3.7 General Purpose Variables**

The following list of variables are ones that can be applied to any combination of Source and Target port. In some instances these variables are meant simply to provide default states for objects in the GUI. In other cases, these variables will have no analogous command line or GUI feature and will affect outputs all on their own.

### **3.7.1 COMMENT**

When using any of the serial protocol formats, this variable will optionally add comments to the patterns That will inform you of the state of the protocol as data is transmitted. These comments will also Be viewable on the target system in the pattern viewers

*Syntax:*

**COMMENT** *ON|OFF*

*Example:*

COMMENT	ON
COMMENT	OFF

### 3.7.2 DDRMODE

In many high speed situations, such as DDR, there will be simulations that have bidirectional pins that go from input to output in a single cycle. The target platform may not be capable of doing this. If a pattern requests this, the end result will be missing input or output data at the DUT. The drivers may not be able to turn on or off in time. If this is the case, you can automatically account for this turn-around issue by applying the affected pins to the following syntax.

*Syntax:*

```
DDRMODE pinName1 [pinName2 ...pinNameN]
```

When DDRMODE is enabled for a given pin or group of pins, the resulting vector data will be automatically modified to account for driver turn around so that important data is not lost due to hardware constraints.

*Example:*

```
DDRMODE DQ DQS MDQ MDQS # turn around issues will be adjusted
```

### 3.7.3 DELAY

In certain instances it may be necessary to move data on a set of pins forward or backward by a number of cycles to get the pattern to match how it will work on silicon. This is done because either the simulation does not match silicon or even because the performance on one source is different than the performance on another target. The DELAY block can be used to adjust the data. The syntax for the block is as follows

#### DELAY

```

    pinName value
    pinName value
    ,
    ,

```

#### END DELAY

*DELAY* is a keyword that indicates the beginning of a DELAY block

Only one *DELAY* block should exist within a given test configuration. No errors will be seen but only the last delay block listed will be inserted into the test program

*pinName* must explicitly match a *PIN* or *ALIAS* defined prior to the *PINLIST* block

*value* will define the cycle count for which data will be delayed for a given pin. Negative numbers will move data forward. Positive values will move the data backward

The example below delays s data pins by 3 cycles, while forcing theCLK to happen 1 cycle early.

```

DELAY
  DATA1  3
  DATA2  3
  CLK     -1
END DELAY

```

### 3.7.4 INIT

In certain instances it may be necessary to apply arbitrary sequences of data to pin that are not defined in the source. These sequences can be made up of any valid vector state characters

#### INIT

```
pinName defaultSequence  
pinName defaultSequence  
,  
,
```

#### END INIT

*INIT* is a keyword that indicates the beginning of a INIT block

*pinName* must explicitly match a *PIN* or *ALIAS* defined prior to the *PINLIST* block

*defaultSequence* will define the state to use instead of whatever state is defined by the source pattern. This will also assign this default state to use when no action is defined by a source pattern. This is useful for applying states to unreferenced pins that need to be biased in a particular way.

```
INIT  
DATA1 0000011111  
DATA2 1010101010  
CLK 110011001100  
END INIT
```

### 3.7.5 PAGE

This directive is used to redefine the number of scan instances that will be included in a single vector file. By default, scan patterns will be broken into separate files that can be bursted together. The reason that these are broken up is because it can make processing and debug easier in that you can mask certain chunks of patterns to make loading quicker.

But, since some patterns don't like the way that bursts are issued, this flag will allow you to make the page size larger or smaller to increase or possibly remove entirely, the need for paging.

PAGESIZE will also be used to define the seed size to use for the paging calculation for VCD/EVCD translation. By default a seed of 1000 cycles is used for this calculation. In some cases, you may want to change the size of pages to address paging issues caused by staggered busses or asynchronous behavior in simulations.

*Syntax:*

**PAGESIZE** *numberPerPage*

*Example:*

```
PAGESIZE      10000  # This will break file every 10,000 scan instances
                # Or a seed value of 10000 for VCD/EVCD files

PAGESIZE      50     # This will break file every 50 scan instances
                # Or a seed value of 50 for VCD/EVCD files
```

### 3.7.6 STATIC

In certain instances it may be necessary to override the termination used for the drive resources that are associated with the read on an IO pin. To drive high or drive low while reading, the termination block is employed. Pins can be set here. If not listed in the termination bloc, a pin will retain its regular Z termination.

#### STATIC

```
    pinName defaultState  
    pinName defaultState  
    ,  
    ,
```

#### END STATIC

*STATIC* is a keyword that indicates the beginning of a STATIC block

*pinName* must explicitly match a *PIN* or *ALIAS* defined prior to the *PINLIST* block

*defaultState* will define the state to use instead of whatever state is defined by the source pattern. This will also assign this default state to use when no action is defined by a source pattern. This is useful for applying states to unreferenced pins that need to be biased in a particular way.

```
STATIC  
    DATA1    0  
    DATA2    0  
    CLK       Z  
END STATIC
```

### 3.7.7 SUBROUTINE

This variable will allow you to determine how subroutines are handled. By default, subroutines will be treated as separate pattern files. But if you turn these off, the calls themselves will be flattened and added directly to the calling pattern.

The default state for this is “ON”

*Syntax:*

**SUBROUTINE** *ON|OFF*

*Example:*

SUBROUTINE	OFF
SUBROUTINE	ON

### 3.7.8 TERMINATION

In certain instances it may be necessary to override the termination used for the drive resources that are associated with the read on an IO pin. To drive high or drive low while reading, the termination block is employed. Pins can be set here. If not listed in the termination bloc, a pin will retain its regular Z termination.

#### TERMINATION

*pinName* *LOW|HIGH*

*pinName* *LOW|HIGH*

,

,

#### END TERM

*TERM* is a keyword that indicates the beginning of a DELAY block

*pinName* must explicitly match a *PIN* or *ALIAS* defined prior to the *PINLIST* block

*LOW|HIGH* will define the state to use instead of Z for the drive action. If the pins is not specifically terminated LOW or HIGH, then it will be terminated to a Z state.

The example below terminates 2 pins low and one pin highy.

```

TERMINATION
  DATA1    LOW
  DATA2    LOW
  CLK       HIGH
END TERM

```

### 3.7.9 TRISTATE

This directive is used to enable and disable the tristate comparison feature. By default, tristate comparisons will be imported as active strobe conditions. If the tristate comparison is turned off, tristate comparisons will be mapped to X's. Turning on the tristate compare is equivalent to leaving the statement out completely.

*Syntax:*

**TRISTATE ON/OFF**

*Example:*

TRISTATE	OFF
TRISTATE	ON

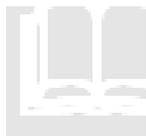
### 3.7.10 WARNINGS

This value is used to allow the user to block highly repetitive warnings that can appear in some translations. If these warnings are deemed to be ignoreable, which they are most of the time, this will block these warnings so the log file is easier to read. By default, warnings are all ON.

**WARNINGS OFF #** Default is on, turns off repetitive warnings

## **3.8 Timing Variables**

The Cyclization Timing section of the Configuration File is used mainly for controlling the conversion of VCD and EVCD patterns, where the stream of events needs to be divided into tester cycles.



**BACKGROUND:** For more information on VCD/EVCD patterns and cyclization, refer to the previous chapter in this guide called “What Happens During the Conversion Process?”, and, specifically, the section called “‘Cyclized’ vs. ‘Uncyclized’ Pattern Formats”.

### 3.8.1 DATARATE

DATARATE refers to the number of ascii vectors that will be expressed per single tester cycle. This variable will provide a default value that can then be overridden by the GUI. Expressing in the CFG will provide a failafe way of defining this so that it is always set when loading a particular CFG.

This variable then sets the maximum data rate that will be used. By default, the same data rate will apply to all ports if more than one port is defined. However, this is only a target. Depending on the relative frequencies of each port, slower ports may be slowed down so that they do not use this value. This is done so that very slow ports are no burdened with the unneeded complexity of a high data rate.

Syntax,

```
DATARATE value
```

Where,

Value = some number between 1 and 8.

EXAMPLE

```
DATARATE 3
```

```
DATARATE 6
```

### 3.8.2 DRIVE Block

When EVCD or VCD files are used as inputs, strobes will be automatically placed at the end of cycles (when snapping is enabled) or at the exact point of transition (when snapping is disabled). Often this is not ideal. The DRIVE block here will allow the user to arbitrarily assign the drive points on a pin by pin basis. Additionally, this will result in spec variables that will be added that can clearly control this from the tester.

*Syntax:*

```
DRIVE
    pinName1    strobeValue
    pinName2    strobeValue
    ...
    pinNameN    strobeValue
END DRIVE
```

Strobe values can be expressed either as raw time values, which default to ns if no units are expressly defined. Alternatively, these can be expressed as % values. In that case, the edge strobe will occur at a particular ratio of the period. Every pin can have its own unique strobe location. Pins that are not defined in the block will have their strobes occur at the regular default location that Velocity calculates.

*Example:*

```
STROBE
    TDO 40% # Strobe the TDO at 40% of the tester period
END STROBE
```

### 3.8.3 EDGES

The EDGES definition specifies the number of “edge-snapping” regions per cycle when “cyclizing” a VCD or EVCD pattern. This corresponds with the **+eN** command-line option for edge snapping resolution and the **Snap Resolution** field in the GUI.

Edge snapping is useful for VCD/EVCD patterns in which the simulation was imperfect and produced edges that varied in time within the clock period from cycle to cycle. Just as many drawing software tools allow a drawn point to “snap” to the nearest grid point, so edge snapping allows an existing edge to be moved automatically to a specific reference time within a cycle.

When edge snapping is enabled for a Velocity conversion, each cycle or period is divided into a number of equal-size regions, as specified by the EDGES definition. Any input edge that falls within a particular snap region will be moved to the earliest time in the region; whereas, any output edge will be moved to the latest time in the region.



**WARNING!** Make sure to specify a number of edges at least as great as the maximum number of edges expected per cycle for any defined Pin. Otherwise, edges will be lost!

For example, if a clock signal exists with two edges – rising and falling – per period, then specify 2 edges. If the number of edges were specified as 1, then both the rising and falling edge of the clock would be snapped to the beginning of the snap region (the period) and the pulse would be lost.

The number of edges specified by the EDGES definition takes precedence over any number of edges specified in a converter command-line option or within the Velocity GUI. This feature helps ensure that the user does not accidentally specify too few snap edges and thus lose edges in the pattern. (See the WARNING above.)

*Syntax:*

**EDGES** *numberOfEdges*

where,

*numberOfEdges* is an integer value

*Example:*

```
EDGES 2
```

### 3.8.4 EQUATION

This directive is used to define whether single or multiple equation sets will be created. SINGLE (common) or MULTIPLE equations 1 per pattern. By default SINGLE mode is used as this produces the smallest and cleanest timing setup. Multiple would be used if the user specifically requires tuning on each pattern to be independent.

*Syntax:*

**EQUATION ON/OFF**

*Example*

```
EQUATION      ON
```

### 3.8.5 NORMALIZE

This variable is used to provide an automatic update to the normalization check box of the GUI or command line. This value can be overridden by the GUI if the box is checked after loading of the CFG. This provides a default value so the user does not have to always remember to check it if desired.

*Syntax:*

**NORMALIZE ON/OFF**

*Example*

```
NORMALIZATION  ON  
NORMALIZATION  OFF
```

### **3.8.6 PERIOD**

The PERIOD definition specifies the time period used for “cyclizing” a VCD or EVCD pattern. A Configuration File can include one or more PERIOD definitions. In the case of multiple definitions, each definition will apply to a different group of Pins to be defined in the subsequent PINLIST block.

Velocity will attempt to divide the VCD/EVCD event stream into the specified period, and determine the resulting drive, tri-state, and compare edge delays within the period.

The period that is specified by a PERIOD definition is also known in Velocity as a **Clock Domain**. The term Clock Domain comes from the fact that devices with synchronous, digital functionality typically have a group of signals whose timing is referenced to a particular clock signal. Therefore, those signals can share the same test system period as the clock. Some devices have multiple clocks operating at different rates, each clock having an associated group of signals synchronized with it. Each group of signals synchronized to a different clock can be said to belong to a separate Clock Domain.

Optionally, each Period / Clock Domain definition can take a name as a second parameter. This name can be used within the subsequent PINLIST block to reference the Clock Domain on a Pin-by-Pin basis. That is, each Pin in the PINLIST can be assigned to a Clock Domain independently of other Pins.

*Syntax:*

**PERIOD** *cycleTime clockDomain*

where,

*cycleTime* ::= *timeValue*[*timeUnit*]

where,

*timeValue* is a numerical value expressed in integer, floating point, or scientific notation

*timeUnit* ::= [*scaleFactor*]**s**

where,

*scaleFactor* is one of the following scaling characters:

**T** means Tera, or 1E12

**G** means Giga, or 1E9

**M** means Mega, or 1E6

**k** means kilo, or 1E3

**m** means milli, or 1E-3

**u** means micro, or 1E-6

**n** means nano, or 1E-9

**p** means pico, or 1E-12

**f** means femto, or 1E-15

*clockDomain* is a character string

*Example:*

PERIOD	1608ps	domain622
--------	--------	-----------



Note: The time value parameter can include units immediately after the number (no whitespace in between). Units can include all the common scaling letters, such as n (for nano), u (for micro), m (for milli), etc. Also note that the name “domain622” has been assigned to the Clock Domain.



Note: There must be a domain name defined for each PERIOD statement. Without the domain assignment the defined period it would never be assigned to any pins.

### 3.8.7 SURROUND

This directive is used to enable or disable the use of surround-by waveforms. By default, surround-by will be enabled. But, there are instances where this is not wanted. For example, sometimes the surround-by will introduce extra edges. Other times, the surround-by will use too many edges. This provides a simple way of disabling the feature if it is not wanted

*Syntax:*

```
SURROUND ON|OFF
```

*Example*

```
SURROUND          ON
```

### 3.8.8 STROBE Block

When EVCD or VCD files are used as outputs, strobes will be automatically placed at the end of cycles (when snapping is enabled) or at the exact point of transition (when snapping is disabled). Often this is not ideal. The STROBE block here will allow the user to arbitrarily assign the strobe points on a pin by pin basis. Additionally, this will result in spec variables that will be added that can clearly control this from the tester.

*Syntax:*

```
STROBE
    pinName1    strobeValue
    pinName2    strobeValue
    ...
    pinNameN    strobeValue
END STROBE
```

Strobe values can be expressed either as raw time values, which default to ns if no units are expressly defined. Alternatively, these can be expressed as % values. In that case, the edge strobe will occur at a particular ratio of the period. Every pin can have its own unique strobe location. Pins that are not defined in the block will have their strobes occur at the regular default location that Velocity calculates.

*Example:*

```
STROBE
    TDO    40%    # Strobe the TDO at 40% of the tester period
END STROBE
```

### 3.8.9 RUNNINGCLOCKS

Free running clocks are pins that are designated as free running and ignore the pattern data during the conversion. Typically these are attached to clock ports (CLOCK). A clock pin will have one of two states, pulse high, 1 or pulse low, 0.

Syntax,

```
RUNNINGCLOCKS
    pinName activeDataState
END RUNNINGCLOCKS
```

Where,

pinName: a pin previously defined in the PINLIST

activeDataState: This will be "0" or "1". "0" means return to one. "1" means return to

zero

EXAMPLE

```
RUNNING_CLOCKS
    CP 1
END RUNNING_CLOCKS
```

## 3.9 Custom Levels



**BACKGROUND:** Simulation output files, and even STIL files, do not typically define DC levels for the signals. However, using configuration file structures, Velocity provides you with a way to include levels information with your auto-generated test program.

The LEVELS block allows you to define, for any pin or group of pins, power supply levels, input drive levels, and output threshold levels.

To define levels for a group of pins, create the following Control definition block.

- On the first line, use the keyword **LEVELS** followed by a pin or group name. Optionally, you can use the word **default** for the pin specification to indicate all pins.
- On the next line, use the keyword **POWER** followed by a voltage value. This will be the master power supply voltage level.
- On subsequent lines, use the following keywords followed either by a voltage value or a percentage:

**VIH** – Input voltage for a logic high

**VIL** – Input voltage for a logic low

**VOH** – Output threshold voltage for a logic high

**VOL** – Output threshold voltage for a logic low



**BACKGROUND:** If you specify a level as a percentage, Velocity interprets it as a percentage of the POWER level. This provides a convenient way to scale levels with a device power supply voltage.

- For the last line, use the keywords **END LEVELS**.

The following is an example of a Levels definition:

```
LEVELS default
POWER 3.0V
VIL 0.8V
VIH 2.0V
VOL 30%
VOH 50%
END LEVELS
```

### 3.9.1 Power Sequences

This section is used to define the power up sequence. Although this section is technically optional, It is strongly suggested that this section be used. Otherwise, the power up will require user intervention in multiple locations in the source files. Syntax of this block is as follows

```
POWER powerStateName
    SupplyName    supplyVoltage  clampCurrent  delayAfter
    SupplyName    supplyVoltage  clampCurrent  delayAfter
    SupplyName    supplyVoltage  clampCurrent  delayAfter
    “”            “”            “”            “”
    “”            “”            “”            “”
END POWER
```

When used, this power sequence can be referenced in the same way that test's (defined next) are used. In other words, this block is treated as a special case of the tests that will allow execution with name pass/fail queries. The power sequence will always result in a pass value and will never log anything.

If a staged power up or power down sequence is required. This can be defined by generating multiple power blocks with unique names for each stage. Or, it can be defined explicitly within a single power block by defining the supply more than once in the block.

- Each entry in the power block is executed serially in the order is defined in the configuration.
- Multiple supplies can be referenced within a single block
- At the end of execution, supplies will retain the supply value last requested

The following is an example of a Power definition:

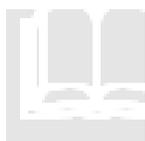
```
#####
# Power up and power down
#####
POWER nominal
    VS1  1.25V  500mA  5uS
    VS2  3.6V   500mA  0uS
    VS3  3.6V   500mA  0uS
END POWER
```

### 3.9.2 Power down sequencing

There will always be a power sequence named “off” created by the ShellConstructor. This default sequence will do nothing more than disconnecting the power supplies. This default sequence will be overridden in the following cases.

- Power off case 1: If only one power up sequence is defined, the power off sequence will be assumed to occur in reverse order. Each supply will be set to 0V and then disconnected in the reverse order of the power up
- Power off case 2: If multiple power up sequences are defined, the power off will default to the reverse order of the last power sequence. Each supply will be set to 0V and then disconnected in the reverse order of the power up
- Power off case 3: If a special power down that is not explicitly equivalent to one of the above, a special POWER block named “off” can be defined that will automatically override the default case. **This is the recommended method**

## 3.10 Custom Timing



**BACKGROUND:** Although Velocity will create appropriate Time Sets for your program, based on the simulation or ATE files used as source for the conversion, you can create your own custom timing to apply to tests.

To define custom timing for a group of pins, create the following Control definition block.

- On the first line, use the keyword **TIMING** followed by a pin or group name. Optionally, you can use the word **default** for the pin specification to indicate all pins.
- On the next line, use the keyword **PERIOD** followed by a time value. This will be the period of the tester’s pattern sequencer.



**BACKGROUND:** All TIMING blocks in a particular Configuration file must use the same PERIOD value. This ensures that the tester will be able to use the resulting STIL file.



**TIP:** In order to use TIMING blocks with different PERIOD values in your test program, use separate Configuration files for each of the different periods and run separate conversions with each.

- On subsequent lines, use the following keywords followed either by a time value or a percentage:

**DRIVE** – Time delay of a drive edge for a pin of type I or IO

**RECEIVE** – Time delay of a compare edge for a pin of type O or IO

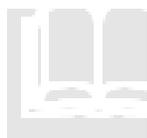
**PULSE** – Duration of a pulsed waveform for a pin that is not defined as a clock pin.

**OFFSET** – Time delay of first edge for a pin of type CLK

**RISE** – Time delay of second edge for a pin of type CLK, if a rising edge

**FALL** – Time delay of second edge for a pin of type CLK, if a falling edge

**DUTY** – Duty cycle for a pin of type CLK, expressed only as a percentage



**BACKGROUND:** If you specify a timing parameter as a percentage, Velocity interprets it as a percentage of the PERIOD time. This provides a convenient way to scale edge delays with a sequencer period.

- For the last line, use the keywords **END TIMING**.

The following is an example of a Timing definition:

```
#####
# Timing
#   These definitions will define the values of specs
#   values will be assigned by default.  Groups and pins can
#   be defined to override defaults by using a pin or group
#   name.
#####
TIMING default
  period 100ns
  offset 0ns
  duty 50%
  drive 25%
  receive 90%
END TIMING
```

### 3.11 TEST Definitions

This section is used to create specific test instances. Each defined test will be accessible from both the main test program and command line execution scripts. The general syntax for the section is as follows. Each entry is then detailed

```

TEST testname testnumber
      TYPE           typeKeyword
      PARM           PARMvalue
      PARM2         PARM2value
      " "             " "
      " "             " "
END TEST

```

**TEST:** Keyword to tell the Velocity that a new test block is being created. This then requires that a unique test name and (optionally) a unique test number to follow. The testname will be the name as accessed by the command line execution script. Each test must have a unique name. The test number will provide a starting testnumber for every element logged. The test numbers should be unique and enough separated from one another so that tests will multiple events will not step on one another.

**TYPE:** The keyword should be the first subparameter of each TEST block. This will tell the Velocity what type of generic function is to be applied. Depending on which parameter type is received, a different set of parameters will then be defined. The typeKeyword can be one of the following values. The parameters that are required for each test type are also defined

- **FUNC:** Functional Test executes a digital pattern and responds with pas/fail results
  - **PATTERN:** Pattern Block name that is to be executed. Note: This pattern name refers to the block name which may be different from the STIL file name that is derived from. The user must know the exact name for this to be valid. This parameters associated value will be case sensitive. Alternatively, "\$default" can be used for the pattern's name and the pattern will be chosen automatically from the input pattern list.
  - **TIMING:** Defines the Timing Block that should be used for a given test.
  - **LEVELS:** Defines the DCLevels Block that should be used for a given test.
  - **ACSPEC:** Defines the Timing Spec category that should be used for a given test.
  - **DCSPEC:** Defines the Level Spec category that should be used for a given test.

- **CONT:** Continuity Test - tests a lists of pins for connectivity by examining voltage seen when small current is applied to pin with no power applied
  - FORCE : Force current value for the continuity test
  - CLAMP: Clamp Value for voltage measurement. This will be the maximum possible voltage that will be received on the active pin
  - LOW: Low value for the continuity voltage measurement
  - HIGH: High Value for the continuity voltage measurement
  - PINS: pin or group name that is to be used for the test. Each pin within a group will be tested individually.
  
- **GONOGO:** Go/NoGO Continuity Test – Essentially identical in setup to the continuity test above. However, in this case, the analog results are not provided and only the pass/fail result of all is determined. This is a faster test than the general purpose continuity
  - FORCE : Force current value for the continuity test
  - CLAMP: Clamp Value for voltage measurement. This will be the maximum possible voltage that will be received on the active pin
  - LOW: Low value for the continuity voltage measurement
  - HIGH: High Value for the continuity voltage measurement
  - PINS: pin or group name that is to be used for the test. Each pin within a group will be tested individually.
  
- **SHRT:** Shorts Test - tests a lists of pins for connectivity by examining current seen when small voltage is applied to pin with no power applied
  - FORCE : Force voltage value for the shorts test
  - CLAMP: Clamp Value for current measurement. This will be the maximum possible current that will be received on the active pin
  - LOW: Low value for the continuity current measurement
  - HIGH: High Value for the continuity current measurement
  - PINS: pin or group name that is to be used for the test. Each pin within a group will be tested individually.
  
- **LEAK:** Leakage Test – Test current leakage on a given pin when particular voltages are applied to the given pin
  - FORCE : Force Voltage value for the leakage test
  - LOW: Low value for the continuity current measurement
  - HIGH: High Value for the continuity current measurement
  - PINS: pin or group name that is to be used for the test. Each pin within a group will be tested individually.

- **IDDQ**: Static IDDQ test. Applies a given functional pattern, stops a given vector location and measures the power supply current at that test point
  - **PATTERN**: Name of functional pattern that is to be used for the given test
  - **PINS**: supply or group of supplies that is to be tested
  - **LOW**: Lowest valid current value that is allowed
  - **HIGH**: Highest possible current value that is allowed
  - **STOP**: comma delimited list of vector numbers or label names that are to be included in the test. This can also refer to a range of numbers by using the dash (“-“). For example, “10,11,12,13” would result in the same set of IDDQ stop locations as “10-13”.
  
- **RELAY**: Relay Open/Close setup. Allows a list of relays to be opened and or closed to provide an arbitrary relay setup that can be referenced by the test’s name
  - **OPEN**: Name of relay pin that is to be opened (optional delay value can be applied to this as well).
    - Example OPEN relay1 10ms ( open relay1 and then wait 10ms)
  - **CLOSE**: Name of relay pin that is to be closed (optional delay value can be applied to this as well).
    - Example CLOSE relay1 10ms ( close relay1 and then wait 10ms)

The following is a sample Test Blocks section that defines a number of tests. Specifically, this list of definitions will result in 8 specifically accessible test Functions defined in TestFunctions.cpp using the generic AC and DC test functions defined in GenericFunction.cpp. There will then be 8 script execution functions defined in user\_commands.cpp. These functions are also available to the Flow Block section of the configuration defined below which can be used to create instances of these functions in a user defined order in the “main” program.

```
#####  
# Test Definitions  
#   The following tests will be defined as discrete functions  
#   that can be executed as user commands or as part of flows  
#   or as modified in C++ user_main.  
#####  
TEST funcSpec 1  
  TYPE      func  
  PATTERN   SpecFunc  
END TEST  
  
TEST shortsPositive 100  
  TYPE      shrt  
  FORCE      10uV  
  CLAMP      1mA  
  LOW        400mA  
  HIGH        800mA  
  PINS       ALL  
END TEST  
  
TEST contNegative 150  
  TYPE      cont  
  FORCE      -10uA  
  CLAMP      2V  
  LOW        400mV  
  HIGH        800mV  
  PINS       ALL  
END TEST  
  
TEST LeakageHi 250  
  TYPE      leakage  
  FORCE      3.6  
  LOW        10uA  
  HIGH        50uA  
  PINS       allin  
END TEST  
  
TEST IDDQ 400  
  TYPE      iddq  
  PATTERN   changeStartStop  
  PINS      vdd  
  LOW        10uA  
  HIGH        50uA  
  STOP        15  
END TEST  
  
TEST IDDQdouble 500  
  TYPE      iddq  
  PATTERN   changeStartStop  
  PINS      vdd  
  LOW        10uA  
  HIGH        50uA  
  STOP        15,16  
END TEST
```

## 3.12 FLOW Definitions

The testflow will insert a predefined set of tests in a particular order into the main program of the test. Each named test or power setting must be defined in prior to use or compilation errors will occur. This is the syntax for the section

```

FLOW flowName
    TEST|POWER|DELAY testname|powerSequenceName|delayValue
    TEST|POWER|DELAY testname|powerSequenceName|delayValue
    ,
    ,
END FLOW

```

*FLOW* is a keyword that indicates the beginning of a flow block

Only one *FLOW* block should exist within a given test configuration. No errors will be seen but only the last flow listed will be inserted into the test program

*testname* and *powerSequenceName* must explicitly match a *TEST* or *POWER* block defined prior to the *FLOW* block

*DELAY* will insert delays in resulting test flow. There must be a number following the *DELAY* statement

The example below assumes that the 2 tests and 1 power sequence have already been defined. The “off” power sequence can either be explicitly defined or implied as being defined because it will automatically be generated because as the reverse of the defined power sequence.

The following is an example of a Flow definition:

```

#####
# Flow Definition
#   The following tests will be executed in the following
#   order.  If no flow is defined, then all the tests will
#   be included in the order they are defined.  All will
#   be called inside user_main
#####
FLOW experimentName
    TEST    contNegative
    POWER   nominal
    TEST    funcSpec
    DELAY   15ms
    POWER   off
END FLOW

```



## **4.0 CUSTOMIZING PATTERNS**



**BACKGROUND:** If your Velocity package includes Optimization options, Velocity can automatically search for compression opportunities when converting patterns, and create appropriate repeats and loops in your STIL patterns.

However, even without Optimization, you can manually customize your pattern files using Configuration file control. With this capability, you can specify explicitly not only repeats and loops, but also selective output masking (pin-by-pin and cycle-by-cycle).

Custom patterns are patterns that are created based on existing patterns but with additional sequencing features such as loops and breaks. By default, every custom pattern will have a base pattern that it is initially created from. After creation, the user can inject an arbitrary list of additional loops and branches to allow for varied execution of the predefined pattern. Therefore, this provides a simple way of automatically introducing modified execution of patterns when it is known beforehand that such changes should occur. Based upon STIL syntax, a number of additions will be made to the output STIL patterns.

First, a new STIL file will be created as a copy of the base pattern. Any labels that are used within the original will be renamed automatically so that they are unique in the copied version.

Second, any new sequences that are requested will be added to the new STIL file. Once compiled, they will be visible to the ITE PatternTool. Eventually, sequencing changes will also be allowed from the PatternTool. But, as of the writing of this document, these features are not yet enabled.

Third, PatternBurst and PatternExec blocks will automatically be created for the new pattern. TEST blocks can then refer to just the pattern name. The PatternExec will be implied. The timing associated with this pattern will be identical to that of the original base pattern. Therefore, no extra work will be required to force timing. This can always be changed but these changes will be made after the Shell is constructed as ITE already has tools to handle this type of activity. The shell, as stated in the introduction, is not meant to be the main user interface. But, rather, it is meant to provide a quick start for new test programs.

## 4.1 Pattern Syntax

The following syntax is used for the PatternBlock

```
PATTERN newPatternName
           BASE      basePatternName
           Command   commandParameterList
           Command   commandParameterList
END PATTERN
```

**PATTERN:** Keyword that tells the ShellConstructor that this is the beginning of a custom pattern block.

*newPatternName:* Must be a unique string to identify the name of the new pattern. This name can be used by subsequent **TEST** blocks.

## 4.2 BASE Syntax

**BASE:** Keyword to indicate that the new pattern is associated with a given base pattern.

*basePatternName:* This base pattern must be included in one of the input STIL patterns to the Shell program. The name of the base pattern must explicitly match the name of the input STIL's **PATTERN** block name.

### 4.3 Command & commandParameterList Syntax

The commands and associated parameters are an optional member of the Pattern Block. However, there will generally be at least one command inserted. Otherwise, there is no real reason to create the custom pattern in the first place. There is no upper limit on the number of inserted commands that can be used. However, when using loops is important that these not be built to interleave. Only one level of looping is defined in this syntax. The following actions can be inserted

#### 4.3.1 TYPE (*optional*)

This optional parameter can be used to determine whether the pattern is to be compiled as a regular pattern or if it is to be defined as a subroutine. (This is only available for the Advantest target port). Other ports will revert to the default type which will compile that patterns as regular functional patterns

**TYPE**    *MAIN/SVEC*

#### 4.3.2 DOMAIN (*optional*)

This optional parameter can be used to lock a set of commands to a particular time domain. If multiple domains are used, then cycle counts that are used to define custom start, stop or loop parameters would need adjustment. This command assigns the reference domain to be used. For the subsequent list of commands

**DOMAIN**    *domainName*

### 4.3.3 FUNC (*optional*)

This optional pattern allows the user to insert a predefined bits stream to particular pin or set of pins. There are a list of predefined bit patterns that can be applied such as PRBS patterns or you can define with a hard path to a file name. This bit stream will be applied to a user defined cycle starting point and can be repeated as any times as desired

```
FUNC patternName[filePath] pinOrGroupName startCycle  
[repeatCount]
```

The pin or group name must be defined above in the pin or group section. The usage of the FUNC keyword must occur after the BASE pattern has been defined. Otherwise, there will be nothing to attach this inserted cycles to. All pins that are not directly referenced by the FUNC statement will be treated as repeats of the previous cycle. If the start cycle is greater than the length of the base pattern, a warning will be thrown and the bit stream will be applied to the end of the pattern. If a repeat count is used and the bit stream itself is not a modulus of the data bit rate, then the pattern will be appended with continuation bits so that it is proper modulus.

### 4.3.4 LOOP

Loops can be added with the following syntax

```
LOOP startCycle,stopCycle [ loopCount ]
```

The start and stop cycle refer to the vector number of the beginning and ending of the inserted loop. A loop count is optional. If not defined, the loop count will be defined as infinite. The loop will have to be stopped by pressing the “abort” button in ITE, as the loop will be interpreted as infinite.

### 4.3.5 REPEAT

Single line repeats can be added with the following syntax

**REPEAT**    *cycle,loopCount*

Cycle defines the vector number for a single line repeat. LoopCount defines the number of times that line should be executed. A loop count of 1 would be equivalent to not having the REPEAT command in the first place.

### 4.3.6 MATCH

Match Loops can be inserted with the following syntax:

**MATCH**    *startCycle,stopCycle [jumpLocation]*

A match loop will execute until the entire range of the loop passes on all cycles. startCycle and stopCycle refer to the vector location of the beginning and the ending for the loop. Optionally, a jump location can be defined with the last argument. If used the pattern execution will jump to the given location after a match is found. If not used, the pattern will continue at the next line

### 4.3.7 START

The start location for a given pattern can be redefined with this syntax:

**START**    *newStartVector*

The start location for a given vector can be redefined with this command. The new pattern will have all previous vector information removed so that the new start location will occur at the vector defined by the parameter newStartVector.

### 4.3.8 STOP

The stop location for a given pattern can be redefined with this syntax:

**STOP** *newStopVector*

The stop location for a given vector can be redefined with this command. The new pattern will have all subsequent vector information removed so that the new stop location will occur at the vector defined by the parameter newStopVector.

### **4.3.9 DELAY**

The DELAY variable will allow you to insert arbitrary time delays at any point in a pattern. These can be inserted at time values or by cycles. If no units are specified for the location it is assumed to be a cycle number

DELAY location[units] duration

### 4.3.10 CUSTOM PATTERN EXAMPLES

The following is an example of a Pattern definition:

```
#####
# Pattern lists
#   The following patterns will be translated.  If the pattern is
#   not in the list, then it will be skipped.  If the pattern is
#   not in the source file then a warning will be issued.
#####
PATTERN loopInfinite
  BASE SpecFunc
  LOOP 5,20
#END PATTERN

PATTERN loopFinite
  BASE SpecFunc
  LOOP 5,18 16
END PATTERN

PATTERN multipleLoop
  BASE SpecFunc
  LOOP 5,10 16
  LOOP 16,20 16
END PATTERN

PATTERN changeStartStop
  BASE SpecFunc
  start 5
  stop 20
END PATTERN

PATTERN PRBS7
  BASE SpecFunc
  FUNC PRBS7  dataIn 800 8
END PATTERN

PATTERN delaysAdded
  BASE SpecFunc
  DELAY 100us  5ms
  DELAY 1ms    2ms
END PATTERN
```

## 4.4 Logical Masking

This keyword will tell the mask loader what command is being requested. These masks are build with a syntax that allows conditional logic to be applied to enable and disable the masking as well as syntax to define how characters are remapping.

Masks can be turned on and off by cycle or pin by pin. **Each command is terminated by a semicolon** at the end of the line. This allows complicated or long statements to be spread over multiple lines

The mask block can also be defined by itself outside of the PATTERN block. In this case the MASK block itself is given a name. If “default” is the name, then the contents of the MASK block are applied to all patterns that are loaded. Any other name will apply the mask only to patterns that match the name of the mask block

```
MASK  default|inputPatternName
        maskCommand maskPinList [map] [conditions]
        maskCommand maskPinList [map] [conditions]
END MASK]
```

It is legal to have both a default and a specifically applied mask for a single pattern. When both are defined, the mask that is specific to the given pattern will be applied first, followed by the default mask block. In the end both are applied. If the input pattern name does not match the name of the mask block, then that mask block is not applied.

#### 4.4.1 PINS

It may be desirable to handle each pins masking separately or collect all masking conditions in a single statement. The syntax is as follows

```
PINS pin1,pin2...pinN start1-stop1,start2-stop2 [condition] [map];
PINS pin1,pin2...pinN start1-END [condition] [map];
PINS pin1,pin2...pinN ALL [condition] [map];
```

In this case, all of the starts and stops for a masking scheme are expressed in a single comma delimited list. Start and stop pairs are separated by the “-“ (dash).

Each start and stop must be an integer that corresponds to a valid cycle number in the loaded pattern. The only exception to the integer limitation is the use of END which all apply the active masked region all the way to the end of a pattern. The other is the use of “ALL”, which will apply the mask to every cycle in the active pattern (Conditions explained below)

#### 4.4.2 MAPS

Character remapping:: By default a mask will take all L, H, and M characters and recast them as X characters. However, the MAP keyword can be used within a mask definition to reassign the state character mappings to any other combination of states. The map conditions specific will override the default. For example, you could use the MAP to turn off drive values. You might even use the map to swap 0 and 1 characters if you want to invert a signal. The MAP is applied with the following sequence

*{MAP=sourceChar|targetChar}*

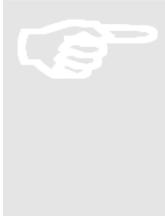
- sourceChar: This can be one or more state characters that might be present in the unmasked source vector.
- targetChar: This can be one or more state characters that would be used to replace the list of characters in the sourceChar listing. If only one character is provided, this character will be applied as the target for all of the states in the sourceChar. If more than one is listed, then the list MUST be the same length as the sourceChar list. The mapping will occur in a 1 to 1 fashion in the same order.

Examples:

{MAP=HM:X} This will turn off all compares

{MAP=01LH:10HL} This will invert all signals, input and output.

{MAP=01LH:ZZXX} This will turn off drives and compares.



Note that the ordering and count of the characters in the the source and target listing for the mask mapping section follows the same convention as STIL waveform tables. The order of the source will match the order of the target. If there is only one target char it will apply to all source chars



Note: Digital Capture can be setup using the MASK block by defining a MAP structure that remaps the L and H characters to C. { MAP [LH:C] } When this is done, the timing will automatically be adjusted to include the capture and don-t capture waveforms

### 4.4.3 CONDITIONS

Mask conditions can be used to fine tune the regions in which a mask is applied so to match conditions in the pattern on any pin at any state prior to the active cycle. Condition sequences will be analyzed as a comma delimited “or” of multiple conditions. Each condition is applied with the following sequence.

*{ COND refPin[relativeCycle]=pinState }*

- **refPin:** This should be an explicit match to a pin in the given pin list. This can be equal to a pin the ON, OFF, or PINS state to which the condition is applied. Or, it may be equal to any other pin in the pin list as defined by the configuration
- **relativeCycle:** This parameter is optional. If no relative cycle is defined, it is assumed to be 0 and will search for the condition on the active cycle that is potentially being masked. This can also be a range of cycles. A positive number will look later in the pattern. A negative number will look at previous cycles.
- **pinState:** This will define that state for the refPin that activates the given mask sequence. If the reference pin is not explicitly equal to the given state, then the mask will be deactivated

#### 4.4.4 EXAMPLES:

PINS clkOut 0-100,1000-END;

- This will turn on masking for the pinNamed clkOut starting at cycle 0 and turning it off at cycle 100. After this the mask will be turn on again at cycle 1000 and will remain active until the end of the pattern because no OFF statement occurs

PINS clkOut 0-100,1000-END {COND RESET=0};

- This will turn on masking for the pinNamed clkOut starting at cycle 0 and turning it off at cycle 100. After this the mask will be turn on again at cycle 1000 and will remain active until the end of the pattern because no OFF statement occurs. Within the active ranges, the mask will only be active if the RESET pin is set to 0. Therefore, if RESET is at any other state during the range, the clkOut pin will not be masked.

PINS clkOut 0-100,1000-END {MAP H:X} {COND RESET[16]=0};

- This will turn on masking for the pinNamed clkOut starting at cycle 0 and turning it off at cycle 100. After this the mask will be turn on again at cycle 1000 and will remain active until the end of the pattern because no OFF statement occurs. Within the active ranges, the mask will only be active if the RESET pin is set to 0 16 cycles prior to the active cycle. In other words, the mask will be active until the RESET pin has been set high for at least 16 cycles. Lastly, Only the H's in the source will be masked. L's will be left alone

## 4.5 Serial Masking

Serial masking is an alternate method for applying arbitrary remappings of character sequences on a given pin. In general, anything that is defined as a serial mask can also be assigned with logical mask syntax as defined above. However, sometimes it is difficult to programmatically define the logical syntax. For that reason the serial masking block was created.

### 4.5.1 SYNTAX

```
GLOBAL MASK pinName1 [pinName2 pinName3 ... pinNameN]
    "sourceString" -> "targetString"
    "sourceString" -> "targetString"
    ...
    "sourceString" -> "targetString"

END GLOBAL
```

The block is initiated and terminated with "GLOBAL MASK" and "END GLOBAL". You can then apply this to one or more pins or groups. These pins or groups must have been defined already in the PINLIST or GROUP blocks.

The source and target strings will define what strings you are searching and replacing. These sequences are searched for vertically on each pin in the listing. If the source string is found, it will be automatically replaced with the target string.

The length of each source string must match the length of its associated target string.

Multiple source and target pairs are executed in the order they are defined inside the block

There can be more than one GLOBAL MASK block per configuration. That way you can assign different combinations of string pairs for different pins.

The serial masking blocks are ALWAYS executed before any logical masking block that has also been created.

## 4.5.2 EXAMPLES

```

GLOBAL MASK DQ DQS DQSb MDQ MDQS MDQSb
"MMMMMMMMMMMMMMMM0" -> "XXXXXXXXXXXXXXXXNNN0"
"MMMMMMMMMMMMMMMMZ0" -> "XXXXXXXXXXXXXXXXNNN0"
"MMMMMMMMMMMMMMMMZZ0" -> "XXXXXXXXXXXXXXXXNNN0"
"MMMMMMMMMMMMMMMMZZZ0" -> "XXXXXXXXXXXXXXXXNNN0"
"MMMMMMMMMMMMMMMMM1" -> "XXXXXXXXXXXXXXXXNNN1"
"MMMMMMMMMMMMMMMMMZ1" -> "XXXXXXXXXXXXXXXXNNN1"
"MMMMMMMMMMMMMMMMMZZ1" -> "XXXXXXXXXXXXXXXXNNN1"
"MMMMMMMMMMMMMMMMZZZ1" -> "XXXXXXXXXXXXXXXXNNN1"
END GLOBAL

```

These will mask turn around for packets that are  
to close together to test

```

GLOBAL MASK DQ DQS DQSb MDQ MDQS MDQSb
"LLL0" -> "NNN0"
"LLH0" -> "NNN0"
"LHL0" -> "NNN0"
"LHH0" -> "NNN0"
"HLL0" -> "NNN0"
"HLH0" -> "NNN0"
"HHL0" -> "NNN0"
"HHH0" -> "NNN0"

"LLL1" -> "NNN1"
"LLH1" -> "NNN1"
"LHL1" -> "NNN1"
"LHH1" -> "NNN1"
"HLL1" -> "NNN1"
"HLH1" -> "NNN1"
"HHL1" -> "NNN1"
"HHH1" -> "NNN1"
END GLOBAL

```